

ATTACHMENT 8

ENGINEERING DEVELOPMENT PROGRAMS

1.0 INTRODUCTION

This attachment contains a summary of the various subsystem engineering development programs being funded by the Program Office. Included is a brief description of the program objectives, status, and scheduled milestones and deliveries.

Bye-108048-70
Page 105

GROUP 1
Excluded from automatic
downgrading and
declassification

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2.0 TRANSDUCERS

2.1 Objectives

The objective of the transducer development program is to develop [redacted] [redacted] designs to the level of confidence required to justify start of System Acquisition in early 1972. Both contractors are assembling and testing large numbers of detectors to verify performance and yield characteristics. In addition, subsystem design studies and hardware implementation of critical components are continuing.

[redacted] has completed the assembly of a [redacted] [redacted] phototransistor array that operates at full system bit rate. The electronic circuitry is primarily of rack and panel construction. [redacted] has re-worked a [redacted] array. The detector elements on the breadboard are at a 0.6 mil pitch. Mechanical and thermal designs for a [redacted] [redacted] will be completed by both contractors during FY 71. Each contractor will complete the assembly of an array of approximately [redacted] by the end of FY 71, the array portion of which will be in flight configuration.

Bye-108048-70
Page 106

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2.2 Testing

Both [redacted] breadboard arrays have been tested in an imaging mode at the Image Processing Laboratory and in flight tests at low altitude. It is planned to perform engineering tests on breadboard arrays from both manufacturers during FY 71. These tests will include the evaluation of the effects of variable detector noise, the requirements for accuracy of detector inter-element calibration, and the various forms of image processing and reconstruction algorithms in the presence of noise, detector miscalibration, and attitude control system instability.

Final reports and experimental test data generated by [redacted] have been prepared as supplements to this documentation package, and are listed in Attachment 13.

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3.0 OPTICS

The objectives of the optical subsystem technology program are to provide analysis and preliminary optical designs for both the Configuration A and B system options during Phase I System Definition, to provide a detailed design of the selected configuration during Phase II System Definition, and to verify the optical element and system tolerances which have been factored into the design and performance prediction tasks via an optical fabrication demonstration. The design and analysis work includes the overall subsystem configuration, structural concept, thermal approach, electrical and telemetry components and interfaces with the Imaging Satellite.

3.1

During Phase I System Definition, the design and analysis studies will emphasize the Configuration B design, as substantial results have already been achieved for a Configuration A design (see references in Attachment 13). The Configuration B design will utilize a diameter aperture and a focal length of . A preliminary report on this configuration will be made in November 1970, with more complete design and performance prediction results to follow in January 1971.

Bye-108048-70
Page 108

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Analysis and limited experimentation will be also performed during Phase I to determine the feasibility, including the impact on cost and schedule for fabrication of the optical subsystem at room temperature and operating at reduced temperature. An initial report on this effort will be submitted in October 1970, followed by the final results in January 1971. A thermal development model will be designed during Phase II.

Interface between the optical subsystem and the transducer will be studied and a specification generated. Preliminary results will be reported in January 1971 followed by complete specifications for the Acquisition Phase. Analyses will be made of both individual and integrated optical and transducer performance testing. A preliminary test plan will be delivered in October 1970 with final plan submittal in January 1971.

The optical demonstration program will produce flight quality optical surfaces on primary and secondary mirrors by December 1970. These elements will then be assembled and tested during Phase II to support the design and performance prediction efforts. Focus and alignment components will also be tested with this assembly.

Bye-108048-70
Page 109

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3.2 Itek

Optical design studies are being conducted by the [redacted] to provide additional analyses of the lens formula, structural configuration and thermal design for the optical subsystem. Results of these studies are scheduled for December 1970. [redacted] is also conducting an optical fabrication program. The objective of this program is to demonstrate a final surface figure of $.02 \lambda$ rms on a $f/2$

[redacted] A multipoint mirror support has been designed and is currently being assembled. This mount will be used during figuring and testing. Concurrent with the conventional fabrication of this mirror, a computer automated optical surfacing machine is being developed and will be used through the final mirror polishing. This machine is scheduled to begin operation during February 1971. Final testing of the finished mirror is scheduled for July 1971.

Bye-108048-70

Page 110

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4.0 RF COMPONENTS

Early in FY 70 [] initiated the development of a breadboard 30 watt traveling wave tube (TWT). The design and performance goals established for the TWT were derived from the communications subsystem studies. The objective of the program was to demonstrate operation of a [] tube in a laboratory setup simulating a typical I/S communications subsystem. The TWT was delivered to [] late in FY 70 and installation was initiated immediately. Initial performance measurements indicate operation within the required values. Table 4-1 summarizes the design goals and the results measured to date. A final report summarizing the test results will be available in September 1970.

After completion of the TWT design, a heater cathode reliability program was initiated. Because of the high frequency and power levels, this tube utilizes a dispenser-type cathode which has been extensively used in high power TWTs. However, none have been space-qualified. Heater cathodes will be life tested in diodes at the nominal and higher-level current densities. The test program will provide sufficient data to proceed with the procurement of flight hardware and result in qualifying sufficient quantities of cathode materials to produce cathodes for many years.

Bye-108048-70
Page 111

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A [] antenna is being designed and fabricated at [] The objectives of this program are the demonstration of the fabrication approach feasibility and the demonstration of high efficiency performance in space-type environment. The [] Cassegrain antenna is being fabricated from graphite epoxy composite material. Both the reflector and subreflector design contours deviate slightly from a parabola/hyperbola in order to achieve higher aperture efficiency. The material characteristics and manufacturing techniques have been selected to achieve and maintain close tolerances on the surface over a temperature range of 250°F. Specific materials and fabrication techniques have been selected and tested, and the analysis and design of the antenna and feed are complete. Assembly of the antenna is complete, with thermal and RF pattern tests scheduled for completion by September 1970. A final report on the antenna performance will be available in October 1970.

Bye-108048-70
Page 112

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TABLE 4-1

TRAVELING WAVE TUBE

PERFORMANCE DATA

<u>PARAMETER</u>	<u>GOAL</u>	<u>TEST RESULTS</u>
Power Output	30 watts (min)	36 to 50 watts
Gain	35 db (min)	30 db at sat. 35 db at 30 watts
Bandwidth	600 MHz (min)	520 MHz
Efficiency	25% (min)	27 - 38% at sat.
Noise Figure	35 db (max)	26 db

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5.0 WIDEBAND DIGITAL RECORDERS

5.1 Objectives

The Program Office is funding a program whose objective is to insure the availability of a magnetic tape digital recorder design which will satisfy the requirements of the I/S, the R/F, and the P/F. The initial program effort involves the development of an engineering model which will demonstrate the design feasibility of a recorder to meet the operational capability required for the I/S flight recorder. Subsequent work will involve the adaptation of this design for use in the R/F and/or P/F.

The recorder design will provide the capability to record and replay digital data at a rate of with a bit error rate of 5×10^{-6} . The tape transport will provide the capability to start and stop within one second. A head/tape interface lifetime of 200 hours is also a key objective. The recorder design will provide for two-year unattended operation with a peak power demand less than 200 watts and a weight less than 200 pounds. Tape interchangeability between all ground recorders is also a requirement for the design.

Bye-108048-70

Page 114

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5.2 Status

Feasibility studies have been completed by both [redacted] has investigated both longitudinal fixed-head and transverse rotary-head techniques. The longitudinal work was entirely analytical, while the transverse work included both experimental and analytical effort. [redacted] has concluded that a transverse recorder design is capable of meeting the requirements with the least development risk. The proposed design would use 8 channels each operating at a rate of 40 Mbps, and incorporate a 32-head, 8-channel headwheel. Experimental tests to date have demonstrated the successful encoding, recording, replay, and decoding of a random 15-bit word repetitive data stream at 20 Mbps. The breadboard design used a variant of Miller encoding and recorded the signal directly on the tape without bias. Best recording performance was obtained at approximately 10 dB below saturation while maintaining a S/N of approximately 30 dB p-p/rms. Time base correction is accomplished by means of digital electrically variable delay lines, which have been tested at rates up to 40 Mbps.

[redacted] has concentrated on the longitudinal fixed-head

Bye-108048-70
Page 115

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design. Their design would incorporate 56 channels on a two-inch tape and utilize a tape speed of 120 ips. This would require recording the data on each track at a density of about 48,000 bpi. Ampex to date has demonstrated packing densities as high as 50 Kbpi with a bit error rate of 5×10^{-5} .

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Page 116

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